

Architecture of the English Electric KDP10 and KDF8 computers.

1. The KDP10.

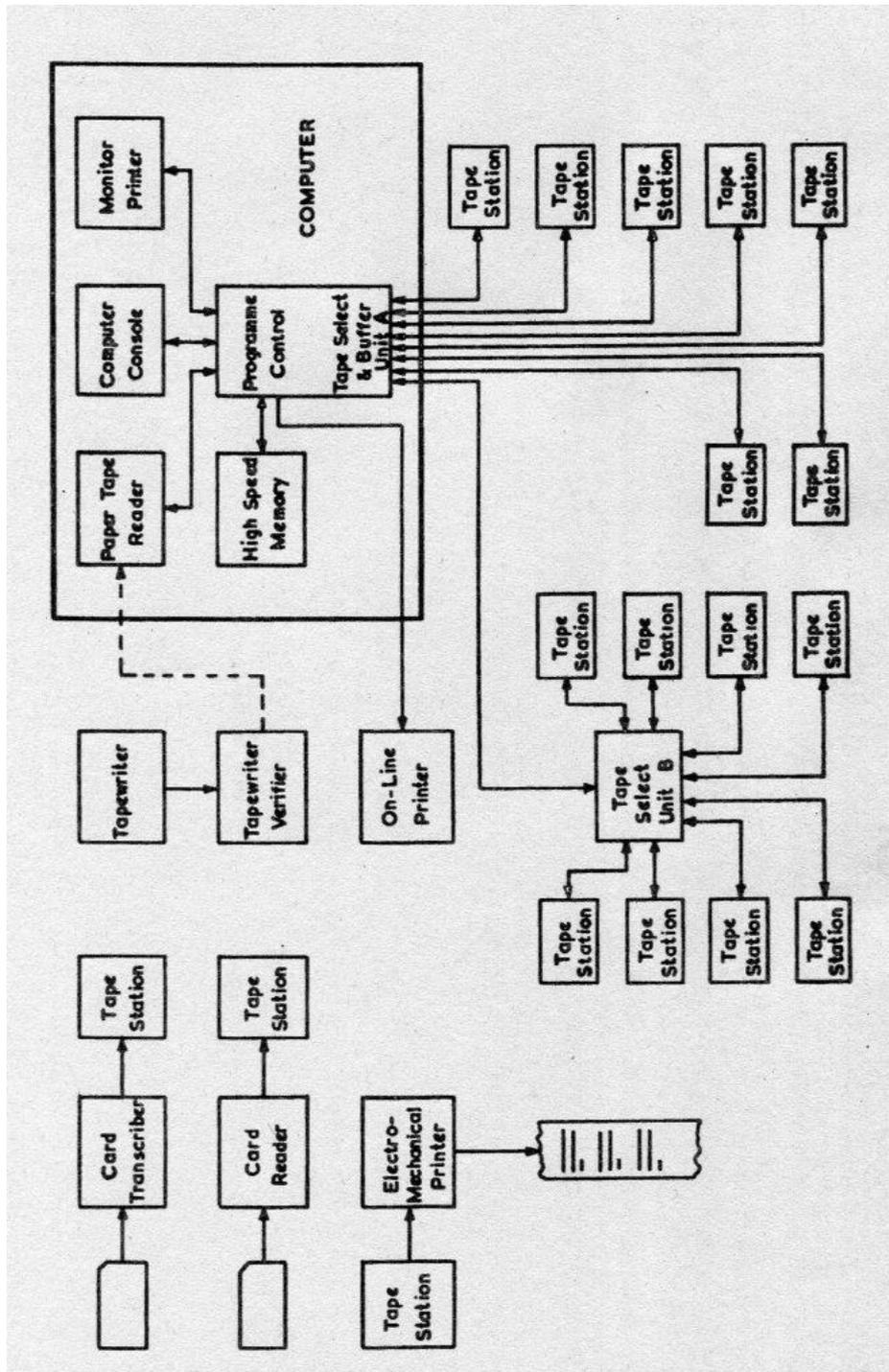


Figure 1. Overall KDP10 system diagram. The above image is taken from: *KDP10 Programming Manual*. English Electric publication 1022. Undated but probably 1961. 198 pages.

Contents of the KDP10-specific information.

- 1.1. KDP10 origins.
- 1.2. KDP10 system overview.
- 1.3. Data representation and variable-length data organization.
- 1.4. Registers.
- 1.5. Address modification and the use of dedicated HSM locations.
- 1.6. Instruction format.
- 1.7. Error-detection and program debugging aids.

*(Information on the **KDF8 computer** follows after section 1.7).*

1.1. KDP10 origins.

The KDP10 was an English Electric version of the American RCA501 computer, intended for commercial data processing. English Electric soon upgraded the KDP10 and re-designated it as the KDF8. Software compatibility was more or less maintained. The first delivery of a KDP10 was in 1962. The first delivery of a KDF8 (or, in at least one case, as an on-site upgrade of a KDP10) was in about 1964.

The RCA 501 was announced in 1958 but had been in development for 'over three years'. It was a medium-to large-scale transistorized machine with printed-circuit boards and a ferrite core primary store (capacity from 16K to 256K characters). Each RCA 501 installation could have up to 63 magnetic tape units. A magnetic drum store was available as an additional option. Input/output was via punched cards or punched paper tape. 501 computers were purchased by the US army and navy and by at least two American insurance companies. . See: <https://www.youtube.com/watch?v=mbV1t0JFyug> of the Computer History Archives project.

1.2. KDP10 system overview.

The English Electric KDP10 computer uses printed circuits, transistors and a ferrite core store (called 'high-speed memory', HSM). The system is expandable with respect to the number of magnetic tape units (known as Tape Stations, see Figure 1), size of primary store and type of peripheral equipment. Up to 62 Tape Stations can be directly addressed by the KDP10 and the whole system design emphasizes magnetic tape as the main (long-term) operational medium. Eight Tape Stations can be connected to Tape Switching and Buffer Unit A (see Figure 1). If more are required, a Tape switching Unit B can be substituted for each of the original eight Tape Stations. Each Tape Station has a unique octal address.

Magnetic tape transfer rates are: 16K or 33 K characters/sec. when writing; 33K characters/sec. when reading. There are 16 channels across the tape, which is $\frac{3}{4}$ inch wide. Each reel of magnetic tape is 2,400 feet in length. Duplicate (ie dual) recording is used, meaning that a single lost bit can be tolerated.

7-track paper tape is used, the paper tape reader operating at 1,000 characters/sec. The paper tape punch operates at either 100 or 300 characters/sec. The Card Transcriber (see Figure 1) reads in 80-column cards at up to 400 per minute and writes the information to magnetic tape. There is a 600 lines/minute Lineprinter.

Higher-speed off-line printing is also available – see the Commercial Union KDP10 given here <https://ourcomputerheritage.org/Maincomp/Eel/N3ExtraCaseStudy.pdf>

Within certain limits, input/output activity and computing activity may proceed simultaneously. The result is that two instructions, one or both of which are input/output instructions, may be executed simultaneously. Instructions are known as Normal Mode (NM) and Potentially Simultaneous (PS). The KDF8 made certain improvements to the arrangements for Simultaneous Mode operation – see sections 2.1 and 2.2 below.

Information within the KDP10 computer is held as binary-coded characters having six information bits and a parity bit. HSM is available in increments of 16K character locations, up to a maximum of 256K character locations, where each location is individually addressable and holds one 6-bit character (plus parity). Either one character or four characters can be accessed in one 15-microsec. cycle. The four-character unit is called a tetrad. The first approximately 164 locations of HSM (addressed as 000000 -> 000243) are reserved locations – (see section 1.5 below).

1.3. Data representation and variable-length data organisation.

Information originating from paper tape, punched cards or magnetic tape is held and processed internally in alpha-numeric character form. The KDP10 instruction set handles variable-length items and every 6-bit character is addressable. Decimal arithmetic as well as binary arithmetic is provided in hardware. Thus, two variable-length decimal items may be added, subtracted, multiplied or divided. Decimal arithmetic is carried out in excess-3 binary code, which has two advantages: simplicity of generating the nines complement of a number; a carry-propagation is the same as with decimal numbers.

The KDP10 is a *true variable* item length system. Use of control symbols and the ability to address each character location individually permit the length of any item in any message to be in strict accordance with that item's actual character count. This allows for total variability of item and message length.

When alphanumeric data is encoded for internal use, five special KDP10 control characters are used as field separators, etc.

<i>Octal</i>	<i>abbreviation</i>	<i>meaning</i>
72	EF	end file
73	ED	end data
74	ISS	item separator symbol
75	EM	end message
76	SM	start message.

In addition, the KDF10's mag tape systems have three special indicators: Beginning of Tape Control (BTC) and End of Tape Warning (ETW) and Physical End of Tape (PET).

A block on magnetic tape consists of eight or more characters, preceded by ISS. A block on (seven-track) paper tape is an even number of characters, equal to or greater than 16, preceded and followed by an inter-message gap.

1.4. Registers.

The KDP10 has some physically-identifiable registers as well as certain reserved HSM locations used in place of explicit registers. For example, HSM locations are used for address-modification (see later). The following eight explicit registers are all addressable:

P register holds the address of the next instruction in sequence.
A register, holds the A part of the instruction.
B register: holds the B part of the instruction
S register: similar to the A register when an operation is in Simultaneous mode.
T register: holds a third address when required; also used as an internal counter.
PRIs: three previous result indicators, each one bit. They indicate whether a result is positive (PRP), negative (PRN) or zero (PRZ).

Note that the following are automatic actions on A and P. STA is an automatic operation which occurs whenever control is to be transferred. STA stores the final contents of the A register in HSM locations 000221 – 000223. STP is an automatic operation which occurs at the end of most instructions. STP stores the contents of the P register in HSM locations 000241 – 000243.

Other (internal) registers include the following.

Memory addressing register: holds the HSM address of the tetrad being processed.

Memory register: holds the tetrad being written to, or read from, HSM.

NO register holds the current op code of the current instruction executed in Normal Mode.

SO register: simultaneous operation. Holds the op code of an instruction in Simultaneous Mode.

N register: holds the N field of the current instruction.

SR register: select read. Holds address of the input device used in a read operation.

SW register: select write. Holds address of the output device used in a write operation.

1.5. Address modification and the use of dedicated HSM locations

A dedicated area of HSM is used in place of separate modifier registers.

<i>Octal digit in the N field</i>	<i>Location of modifier</i>
0	No modifier
1	HSM locations 000111 -> 000113
2	HSM locations 000221 -> 000223 (STA)
3	HSM locations 000131 -> 000133
4	Use the P register
5	HSM locations 000151 -> 000153
6	Use the T register
7	HSM locations 000171 -> 000173

Below is a summary of standard HSM locations used for dedicated purposes.

HSM locations	Use
000001 – 000003	The Return After Interrupt (RAI) instruction uses these.
000004 – 000017	Used as temporary space by arithmetic instructions
000020 – 000037	Used by read and write instructions
000040 – 000047	Rollback entrance, normal.
000050 – 000057	Rollback entrance, simultaneous mode.
000111 – 000173	Used for address modification (see separate table)
000200	Control transferred to this address if a Paper Advance is sensed (SSM instruction) in the Simultaneous Mode
000221 – 000223	STA and AM2
000241 – 000243	STP

1.6. Instruction format.

The KDP10's repertoire consists of 49 separate instructions. Each instruction is eight characters (16 octal digits) long and is in the two-address format. Instructions are stored in HSM in two successive tetrads. Instruction-fetch therefore takes 30 microseconds (two memory cycles). The instruction layout is:

<op code> <A-address> <N code> <B address> , where:

- <op code> = two octal digits
- <A-address> = six octal digits; usually a High Speed Memory (HSM) address of an operand (tetrad) or the left boundary of an operand.
- <N code> = two octal digits; permitting automatic modification of an A- and/or B- address via any of the seven (four static and three dynamic) Address Modifiers.
- <B-address> = six octal digits; usually a HSM address of an operand (tetrad) or the right boundary.

Information on the times of both KDP10 and KDF8 instructions are given below in section 2.4. For more information and the complete list of KDP10 instructions, see *Our Computer Heritage* section N3X3.

1.7. Error-detection and program debugging aids.

Many error-detection facilities are incorporated into the KDP10. Arithmetical operations are checked by repeat operations using the complements of the operands. Information-transfers are checked by parity. Breakpoints, to aid program debugging: there are six two-positional ('active' or 'ignore') breakpoint switches on the KDP10's console. Rollback is provided upon error-detection. Rollback is a pre-stored subroutine which is automatically entered when a parity error is detected

during magnetic tape operations. The interrupted instruction is then automatically repeated. Rollback may be inhibited by a console switch.

2. The KDF8 computer.

Contents.

- 2.1. General.
- 2.2. Registers.
- 2.3. KDF8 instructions.
- 2.4. KDF8 and KDP10 instruction times.

The information comes mostly from: *KDF8 Programming Manual*. English Electric publication 1023, 47 pages. Deduce that the publication date was about 1965.

2.1. General.

The KDF8 was marketed as a program-compatible replacement for the KDP10, whilst giving significant [sic] improvements in performance. The KDF8's ferrite core store, known as High Speed memory (HSM), has a cycle time of 12.5 microsecs. whereas the KDP10's cycle time is 15 microsecs. Read or Write transfers between the KDF8 computer and its magnetic tape decks is at the rate of 40K characters/sec., whereas the figures for the KDP10 are: 16K or 33 K characters/sec. when writing; 33K characters/sec. when reading. In all other respects, there is full compatibility between the magnetic tape units (known as Tape Stations) of the KDP10s and KDF8s.

The punched card and paper tape equipment available with the KDF8 computer is similar to the devices available for the KDP10. In addition, superior performance lineprinters, particularly the model 1040, are available for the KDF8. The model 1040 provides 1,000 lines/minute and 80, 120 or 160 characters per line. In a change from the KDP10, information to be printed on the model 1040 is laid out as if being written to magnetic tape using tape-writing instructions and the appropriate trunk number.

In the KDF8 there has been an enhancement to the Simultaneity, or so-called 'time-sharing', features. Simultaneity for the KDP10 is defined as 'coincident execution of two instructions, both or one of which is an input-output instruction'. This is known as SIMO 1. The KDF8 includes an 'additional simultaneous mode', which allows read/write/compute to be achieved. This is known as SIMO 2. There are consequential changes in the KDF8 to certain registers and the detailed operation of certain instructions.

2.2. Registers.

The following KDF8 central registers are identical to those found in the KDP10: P register, A register, B register, T register, PRIs, Memory addressing register, Memory register, NO register, N register, SR register, SW register. Their purpose is as described in section 1.4 above.

The KDF8 has the following new registers:

S0: a one-character register holding the op code of the read instruction when the read is executed in SIMO 1 mode.

S1: a three-character register holding the A address of a read instruction when the read is executed in the SIMO 1 mode.

S2: ditto, holding the A address of a write instruction when the write is executed in the SIMO 2 mode.

SC: a one-character register used as temporary storage (used in place of SR or SW). This register is also used for Break Point recognition on a transfer of control instruction and for decoding the Store Register and Set Register instructions.

A, B, P, S1, S2 and T are all addressable registers.

2.3. KDF8 instructions.

Most of the KDF8 instructions are exactly the same as those of the KDP10. These are given in full in *Our Computer Heritage* section N3X3. However, as explained more fully in N3X3, the exact operation of about 12 of these instructions has been slightly altered for the KDF8. Furthermore, there are two completely new instructions in the KDF8's repertoire, as follows:

- 60 sense simultaneous operations.
- 74 control simultaneous gates 1 & 2.

The format of all instructions remains as described in section 1.6 above. Note that, as before, the following are automatic actions on A and P registers. STA is an automatic operation which occurs whenever control is to be transferred. STA stores the final contents of the A register in HSM locations 000221 – 000223. STP is an automatic operation which occurs at the end of most instructions. STP stores the contents of the P register in HSM locations 000241 – 000243.

2.4. KDF8 and KDP10 instruction times.

Detailed formulae for calculating the time for each KDF8 instruction is given on page 39 of the *KDF8 Programming Manual*. Some sample instruction times are given below. For comparison, the KDP10 times are also given in the Table. The differences in time between the two computers are the result of differences in the ferrite core store cycle times.

In the expressions that follow:

- t = number of characters transferred;
- n1 = total number of spaces and/or minus characters occurring to the right of both operands;
- n2 = number of digits in the shorter operand;
- n3 = difference in number of digits of the two operands;
- x = number of chars in the augend or the operand to be modified in a logical operation.

y = number of digits in the result.

Then, for KDP10, if result is negative, add $25(y+1) + 12.5$ microsecs. Or, for KDF8, if result is negative, add $30(y+1) + 15$ microsecs.

Op code	Function	STA?	KDP10 basic time*, in microseconds	KDF8 basic time*, in microseconds.
21	Item transfer	Yes	30t	25t
41	Binary add	Yes	45x	37.5x
47	Logical AND	Yes	45x	37.5x
51	Decimal add	Yes	$15n_1 + 45n_2 + 30n_3 + 90$	$12.5n_1 + 37.5n_2 + 25n_3 + 75$
61	Conditional transfer of control	No	If zero path taken, then staticising time only. If + or – path taken, then 15	If zero path taken, then staticising time only. If + or – path taken, then 12.5
71	Transfer of control	No	15	12.5
72	Set register	Only if A reg set	15	12.5

* It is necessary to add certain extra times to the basic times given in the above Table, as follows.

- (i). Staticising time (also known as *instruction-fetch time*) of 25 microsec (KDF8) or 30 microsec. (KDP10) is constant for each instruction. This time consists of two memory cycles, during which the two tetrads (ie eight octal digits in all) which make up an instruction are fetched from the HSM.
- (ii). Automatic address modification time of 25 microsec. (KDF8) or 90 microsec. (KDP10) If either the A or B address is to be modified; or 50 microsec. (KDF8) or 180 microsec. (KDP10) if both addresses are modified;
- (iii). STA time of 12.5 microsec. (KDF8) or 15 microsec. (KDP10), for certain instructions.

STA is an automatic operation which occurs whenever control is to be transferred. STA stores the final contents of the A register in HSM locations 000221 – 000223. STP is an automatic operation which occurs at the end of most instructions. STP stores the contents of the P register in HSM locations 000241 – 000243.